REMARKS/ARGUMENTS

Claims 1-25 are pending in this application. Claims 1, 4, 8, 13 and 23 have been amended without adding any new matter. Reconsideration of the application in view of the above amendment and the following remarks is respectfully requested.

35 U.S.C. 103 Rejection of Claims 1-25

The Examiner has rejected claims 1-5, 8-10, 12-17, 23 and 25 under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. Patent No. 6,120,301 to Ichitani et al. (hereinafter "Ichitani") in view of U.S. Patent No. 5,396,104 to Kimura. Applicant respectfully traverses the rejection on the grounds that neither Ichitani nor Kimura alone or in combination provide a factual basis for a *prima facie* case of obviousness.

The Ichitani patent discloses a semiconductor package including a microchip (12) disposed on a substrate. Wires (23) connect bond pads on the chip (12) to terminal pads or internal terminals 12 on top surface of the substrate. Additionally, Ichitani shows external terminals 13 formed on lower surface of the substrate. The internal terminals 12 and the external terminals 13 are electrically connected together through the electric wires 14.

Clearly, Ichitani fails to disclose the feature of directly electrically connecting any of the terminal pads to any of the coated bonding pads with the pre-insulated bond wires, as recited in amended independent claims 1 and 8. As clearly shown in Fig. 1a, Ichitani shows only one row of terminal pads on the substrate and one row of electrode pads corresponding to the terminal pads. In column 7, line 52 to column 8, line 8, Ichitani discloses forming a row of electrode pads on the chip and placing the chip on the wiring substrate. However, in this type of configuration, only a specific terminal pad can be electrically connected to a specific bonding pad. In other words, the bonding pads of the chip are aligned with the terminal pads of the substrate in Ichitani, such that adjacent wires connecting the terminal pads to bonding pads are generally parallel to one another. In fact, this type of parallel configuration is described as a prior art on page 14 of the specification. In this parallel alignment, the wires will never crossover one another and will thus never come in contact with each other. This is because in Ichitani such a contact will cause short circuit problems since these wires are not insulated prior to connecting them to the electrode and terminal pads. Whereas, in the present invention, the wires are insulated prior to connecting any of the terminal pads to any of the bonding pads as recited in amended independent claims 1 and 8. Furthermore, Ichitani fails to show a plurality of bond pads in a plurality of rows and columns over the surface of the chip as recited in amended independent claim 8.

The Examiner alleges that Ichitani shows all of the elements of the claims except the method of forming a semiconductor package including providing and attaching pre-insulated bond wires as claimed by the Applicant, which he alleges is disclosed by Kimura. The Examiner then alleges that it would be obvious to one of ordinary skill in the art to modify the bonding process of Ichitani by using pre-insulated bond wires as taught by Kimura to produce reliable semiconductor devices that are easy to manufacture.

Contrary to Examiner's assertion, Kimura fails to show the method of forming a semiconductor package including attaching pre-insulated wires in the manner recited in amended independent claims 1 and 8.

The Kimura patent discloses a method of manufacturing a bonding wire including coating the same with an insulation film. Kimura further suggests that a semiconductor device may employ these insulated bonding wires. However, Kimura fails to disclose or suggest the method of packaging a high-density integrated circuit by directly connecting or attaching pre-insulated bond wires between any of the terminal pads and any of the coated bonding pads as recited in amended independent claims 1 and 8.

Neither of the references Ichitani nor Kimura alone or in combination teach or suggest electrically connecting any of the bonding pads with any of the terminal pads with the pre-insulated bond wires as claimed in amended independent claims 1 and 8. Therefore, it is respectfully submitted that amended independent claims 1 and 8 and claims 2-7 and 9-12 that depend on claims 1 and 8 respectively, are patentable over the combination thereof.

Referring to amended independent claims 13 and 23, Ichitani fails to disclose the feature of electrically conductive via holes connecting said terminal pads directly to connectors on an opposite side of said substrate. Additionally, Ichitani also fails to disclose the feature of the substrate being sized and shaped to provide number of rows of terminal pads and associated said via holes so that horizontal traces through said substrate are not required as recited in amended independent claims 13 and 23.

As clearly shown in Fig. 1a, Fig. 1b, Fig. 4a, Fig. 4b and disclosed in column 5, lines 30-32, Ichitani states "the internal terminals 12 and the external terminals 13 are electrically connected through the electric wires 14." Whereas, as disclosed and claimed in the present invention, the terminal pads are directly connected to the connectors via electrically conductive holes. There is no wiring required in the present invention to connect the terminal pad to the connector.

In column 5, lines 32-27, Ichitani continues to state "A number of electric wires 14 that are electrically insulated from each other are patterned in each of the layers of the base 11 formed in a multi-layer structure, the upper layers and the lower layers being connected together through holes thereby to constitute a so-called multi-layer wiring structure." This multi-layer wiring structure clearly indicates that horizontal traces are required in Ichitani to pattern the wires in each layer and further connect the multiple layers.

Whereas, in the present invention, each bond pad is directly connected to an individual terminal pad via an insulated bond wire and each terminal pad is connected to the individual connector via an electrically conductive hole. So, the substrate is sized and shaped to provide number of rows of terminal pads and its associated via holes such that each and every electrical signal accessible through a bond pad is available at a connector without any horizontal traces.

The Examiner alleges that Ichitani shows all of the elements of the claims except the method of forming a semiconductor package including providing and attaching pre-insulated bond wires as claimed by the Applicant, which he alleges is disclosed by Kimura. The Examiner then alleges that it would be obvious to one of ordinary skill in the art to modify the bonding process of Ichitani by using pre-insulated bond wires as taught by Kimura to produce reliable semiconductor devices that are easy to manufacture.

Contrary to Examiner's assertion, Kimura fails to show the integrated circuit package and method of manufacturing the same in the manner recited in amended independent claims 13 and 23.

As discussed above, the Kimura patent discloses a method of manufacturing a bonding wire including coating the same with an insulation film and further employing these insulated bonding wires in a semiconductor device. However, Kimura fails to disclose, teach or suggest the integrated circuit package having electrically conductive via holes to connect the terminal pads on the substrate directly to the connectors on an opposite side of the substrate as recited in amended independent claims 13 and 23. Furthermore, Kimura also fails to disclose, teach or suggest the integrated circuit package having a substrate being sized and shaped to provide a sufficient number of rows of terminal pads and associated said via holes so that horizontal traces through the substrate are not required, as recited in amended independent claims 13 and 23.

Neither of the references, Ichitani nor Kimura, alone or in combination, teach or suggest the feature of electrically conductive via holes and substrate being sized and shaped with sufficient number of rows of terminal pads with said via holes so that horizontal traces through the substrate are not required as claimed in amended independent claims 13 and 23. Therefore, it

is respectfully submitted that amended independent claims 13 and 23 and claims 14-22 and claims 24 and 25 that depend on claims 13 and 23 respectively, are patentable over the combination thereof.

Moreover, there is no motivation or suggestion in either reference to modify the bonding process of Ichitani by using pre-insulated bond wires taught by Kimura as proposed by the Examiner. Kimura discloses providing pre-insulated wires to prevent short circuit when the wires come in contact to each other (see column 5, lines 11-14 and column 14, lines 1-5). As discussed above in Ichitani, the bond wires are connected in a parallel configuration on top of the substrate with multi-layer wiring on the bottom of the substarte . Since the wires in Ichitani never touch one another on top of the substrate , there would be no purpose or need to use the pre-insulated wires of Kimura in Ichitani's device. Further, insulating the wires on top of the substrate would not serve any purporse since the semiconductor device of Ichitani can function without such an insulation. In fact to do so would be contrary to Ichitani's intent and purpose. This is simply because in Ichitani, the semiconductor device is intentionally manufactured to align each bond pad on the chip with a corresponding terminal pad on top of the substrate to create a parallel alignment of the wires, thereby connecting the bond pad to its corresponding terminal pad. So, insulating these wires in Ichitani prior to manufacturing the device will clearly

destroy its intent and purpose to align the bond pads on the chip to the terminal pads on the substrate in the manner discussed above.

Therefore, as discussed above, there would be no motivation to combine the references in the manner suggested by the Examiner and so the references are not properly combinable. However, even if the references were properly combinable, such a combination would still lack the teaching of the substrate not requiring any horizontal traces and the teaching or suggestion of connecting any one of the terminal pads on the substrate to any one of the bonding pads on the chip. Thus, it is submitted that amended independent claims 1, 8, 13 and 23 and claims dependent there from are patentable over the combination thereof.

The Examiner has rejected claims 6, 7 and 11 under 35 U.S.C. §103(a) as being allegedly unpatentable over Ichitani in view of Kimura and further in view of U.S. Patent Publication 2002/0045290 A1 to Ball. Additionally, the Examiner has rejected claims 18-20 and 24 under 35 U.S.C. §103(a) as being allegedly unpatentable over Ichitani in view of Kimura and further in view of U.S. Patent No. 5,471,010 to Bockelman et al. Finally, the Examiner has rejected claims 21 and 22 as being allegedly unpatentable over Ichitani in view of Kimura and further in view of U.S. Patent No. 4,002,282 to Murdoch. Applicants respectfully traverse these rejections.

These references in combination reject dependent claims 6, 7, 11, 18-20, 21, 22 and 24 that depend on independent claims 1, 8, 13 and 23 and incorporate by reference, all the features thereof. Since amended independent claims 1, 8, 13 and 23 are patentable over the prior art, as discussed above, applicants submit that the dependent claims 6, 7, 11, 18-20, 21, 22 and 24 are allowable for the same reasons as advanced allowability of claims 1, 8, 13 and 23.

In view of the amendment and remarks above, Applicant deems this application to be in condition for allowance and solicits such action. In the event that any issues remain following entry of this amendment, Applicant's agent respectfully invites the Examiner to contact the

undersigned agent at the telephone number given below for either a personal or telephone interview if the Examiner believes that such would expedite the prosecution of this application.

Respectfully submitted,

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